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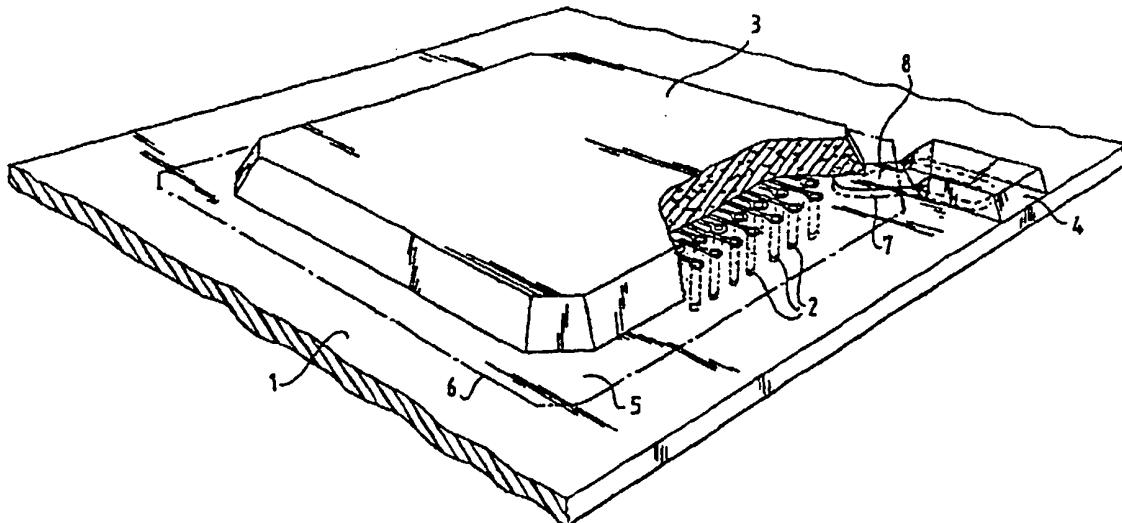
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(54) Title: METHOD, CARRIER AND MOULD PARTS FOR ENCAPSULATING A CHIP



(57) Abstract

The invention relates to a method for encapsulating a chip placed on a flat carrier (1), on one side of which is arranged the chip for encapsulating and on the other side of which are arranged the connection points distributed in a grid structure over the carrier (1), by: placing the carrier between two mould halves (9, 10) movable between an opened and a closed position and bounding a mould cavity in the closed position, and transporting encapsulating material (3) from a supply device to a mould cavity through a channel (7, 15) arranged in the carrier (1).

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METHOD, CARRIER AND MOULD PARTS FOR ENCAPSULATING A CHIP

The invention relates to a method for encapsulating a chip placed on a flat carrier, on one side of which is arranged the chip for encapsulating and on the other side of which are arranged the connection points distributed in a grid structure over the carrier. The invention also relates to a carrier of the stated type and mould parts for encapsulating a chip according to the said method.

Since the carrier referred to in the preamble (also known as "ball grid array board") is larger than the moulding for producing, it is probable that with application of the conventional technique for encapsulating chips a quantity of encapsulating material from the runner remains adhered to the edge of the carrier. This is undesirable because a local thickening of the edge of the carrier can be disadvantageous for the further use of the carrier with encapsulated chip. In order to prevent such a local thickening in the edge of the carrier, use is presently made of a mould consisting of at least three mould parts. Such a mould has the important drawback however that automated operation of such a mould is difficult. Another drawback is a comparatively complex and therefore expensive construction of the mould.

The present invention therefore has for its object to provide a relatively simple method for encapsulating a chip on a carrier of the stated type. The invention has the further object to provide mould parts and a carrier suitable for applying this method.

The invention provides for this purpose a method for encapsulating a chip as according to the preamble by:

placing the carrier between two mould halves movable between an opened and a closed position and bounding a mould cavity in the closed position, and transporting encapsulating material from a supply device to a mould cavity through a channel arranged in the carrier.

The invention further provides a carrier characterized by a channel arranged in the carrier, and mould parts for use

with this method. With these steps a feed runner is arranged in the carrier. This feed runner therefore no longer has to be accommodated in the mould parts, whereby the whole mould can be embodied simply. A mould consisting of two mould 5 halves is now a possibility, whereby automation of the moulding is possible. The mould parts can also be less complex in manufacture and thus less costly. Wear of the mould parts and danger of leakage is also limited herewith.

A preferred embodiment of the carrier is characterized 10 in that the channel in the carrier is formed by a groove arranged on one side in the carrier. Another preferred embodiment of the carrier is characterized in that the channel arranged in the carrier is an elongate opening in the carrier. The groove in particular limits wear to the mould 15 and simplifies very considerable the construction of the mould. The elongate opening has the advantage that less fluid encapsulating material can also be carried to the mould cavity without the capacity of the feed runner forming a limitation. Due to the elongate opening it is also possible 20 to supply the encapsulating material from a chosen side.

The following invention will be further elucidated with reference to the non-limitative embodiments shown in the following figures. Herein:

Fig. 1 shows a partly cut away perspective view of a 25 flat carrier on one side of which is arranged the encapsulated chip and on the other side of which are arranged the connection points distributed in grid structure over the carrier, wherein a part of the encapsulating material is received in a channel arranged in the carrier,

30 Fig. 2 shows a partly cut away perspective view of the carrier of fig. 1 in cut-out situation,

Fig. 3 shows a cross section through a carrier placed between two mould halves, wherein the channel is in a groove located in the carrier, and

35 Fig. 4 is a cross section through a carrier wherein the channel is an elongate opening.

Fig. 1 shows a carrier 1 on which are arranged on one side a chip (not shown here) and on the other side connection points 2 in grid pattern. An encapsulating material 3, for

instance an epoxy resin, is arranged round the chip 1. A material portion 4 formed by a runner in the mould half can also be seen on the edge of the carrier 1. In order to obtain, after cutting out the encapsulated chip, a remaining 5 carrier part 5 designated with the dashed line 6 and having an edge thickness the same throughout, a feed runner 7 for encapsulating material is arranged in the carrier 1. As shown clearly in fig. 2, after arranging of the encapsulating material 3 the feed runner 7 is filled to the same height as 10 the encapsulating material 8 filling the upper part of the carrier part 5.

Fig. 3 shows two mould parts 9, 10 wherein a plunger 11 arranged in the lower mould part 10 by means of heating and applying pressure to a pallet 12 urges encapsulating material 15 through a runner 13 in the upper mould part 9 and then through the runner 7 arranged in the carrier 1 to a mould cavity 14.

Fig. 4 shows a carrier 1 wherein a groove-like opening 15, here filled with encapsulating material, forms the 20 channel arranged in the carrier 1. The groove-like opening 15 can be supplied on a chosen side.

CLAIMS

1. Method for encapsulating a chip placed on a flat carrier, on one side of which is arranged the chip for encapsulating and on the other side of which are arranged the connection points distributed in a grid structure over the carrier, by:

placing the carrier between two mould halves movable between an opened and a closed position and bounding a mould cavity in the closed position, and

10 transporting encapsulating material from a supply device to a mould cavity through a channel arranged in the carrier.

2. Carrier for a chip, on one side of which is arranged the chip for encapsulating and on the other side of which are arranged the connection points distributed in the grid structure over the carrier, for use in a method as claimed in claim 1, characterized by a channel arranged in the carrier.

3. Carrier as claimed in claim 2, characterized in that the channel arranged in the carrier is a groove arranged on one side of the carrier.

20 4. Carrier as claimed in claim 2, characterized in that the channel arranged in the carrier is an elongate opening in the carrier.

5. Mould parts for use with a method as claimed in claim 1.

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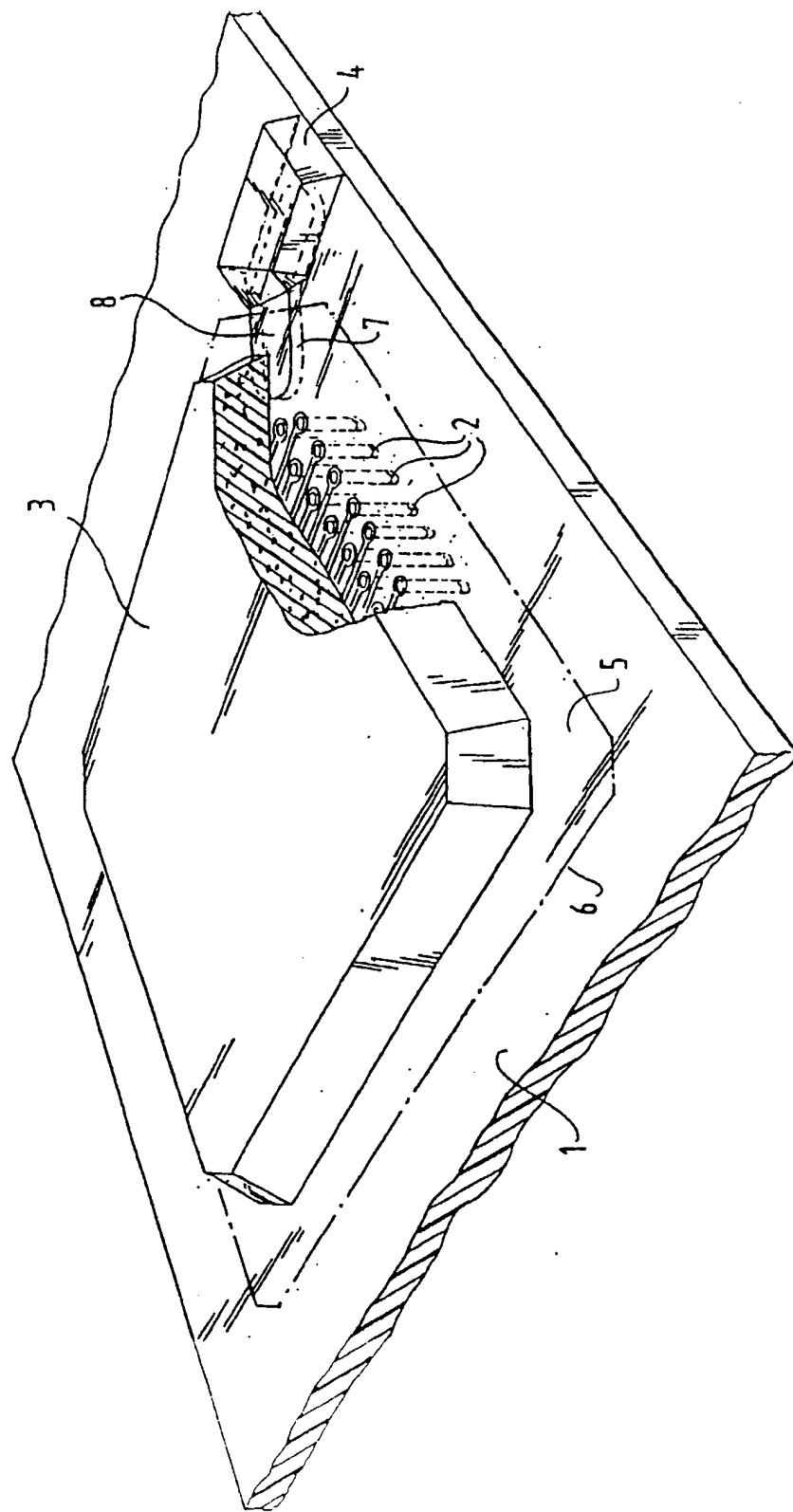


FIG. 1

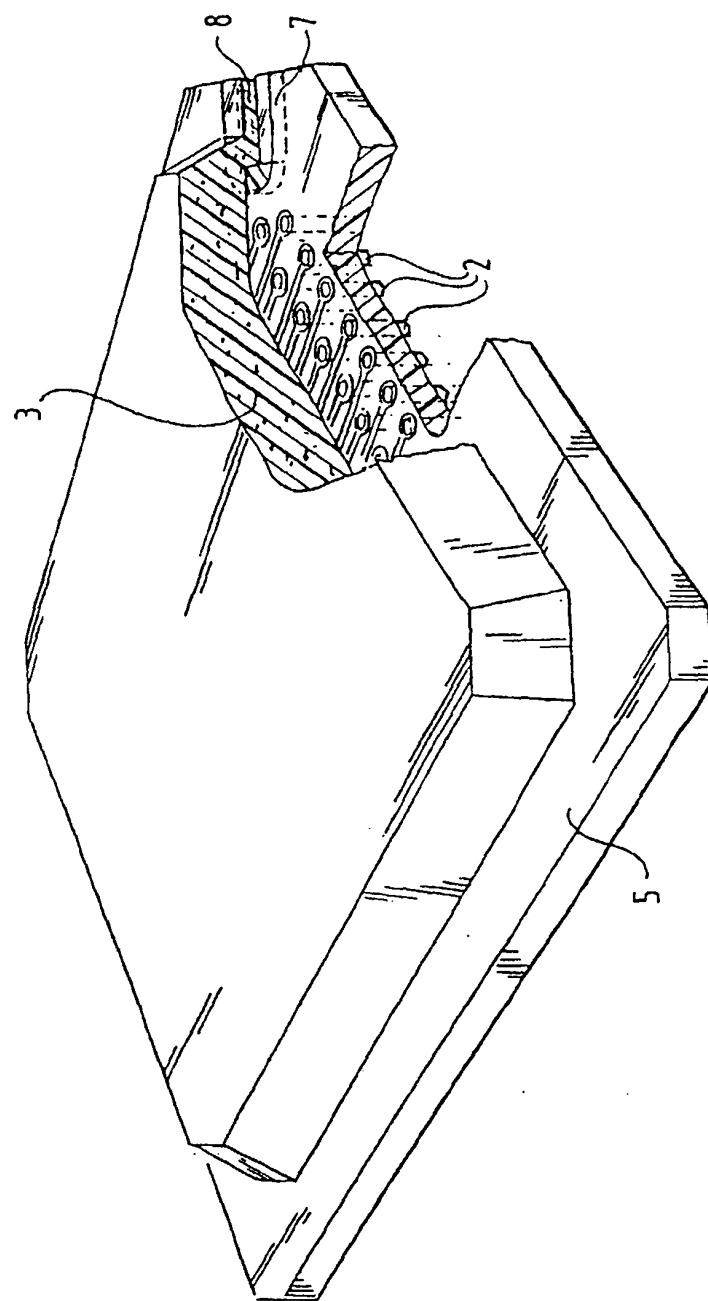
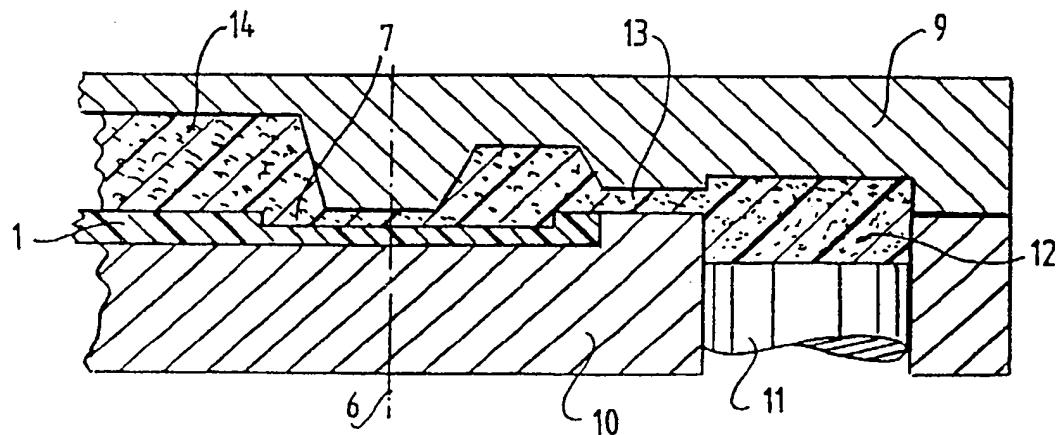
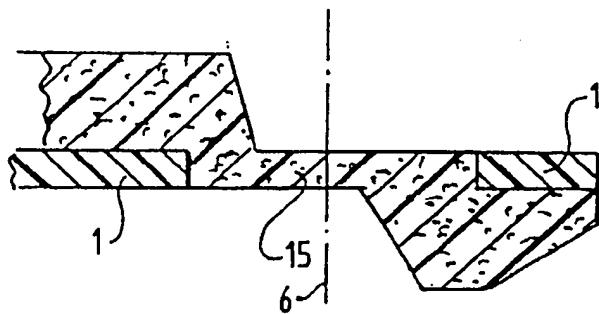


FIG. 2

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FIG.3FIG.4

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/56

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GB-A-2 218 570 (NAT SEMICONDUCTOR CORP) 15 November 1989 see the whole document ---	1,2,4,5
X	PATENT ABSTRACTS OF JAPAN vol. 013 no. 235 (E-766) ,30 May 1989 & JP,A,01 041254 (NEC CORP) 13 February 1989, see abstract; figure 2 ---	1,2,4,5
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Date of the actual completion of the international search	Date of mailing of the international search report
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INTERNATIONAL SEARCH REPORT

Internat'l Application No
PCT/NL 95/00232

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X	PATENT ABSTRACTS OF JAPAN vol. 017 no. 137 (E-1335) ,22 March 1993 & JP,A,04 306865 (SEIKO EPSON CORP) 29 October 1992, see abstract ---	1,2,4,5
X	PATENT ABSTRACTS OF JAPAN vol. 010 no. 137 (E-405) ,21 May 1986 & JP,A,61 001067 (STANLEY DENKI KK) 7 January 1986, see abstract -----	1,2,4,5

INTERNATIONAL SEARCH REPORT
Information on patent family members

Int'l Appl. No.
PCT/NL 95/00232

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